Amendments to the Specification:

Page 1, please replace the first two paragraphs as follows:

IGFET and Tuning Circuit

Background of the Invention

Field of the Invention

The present invention relates to an insulated gate field effect transistor and a tuning circuit.

~~**Background to the Invention**~~
Description of the Prior Art

LC tuned circuits are widely used in RF circuits, such as oscillators and tuned amplifiers. It is often necessary, for instance in multiband radio equipment, to change the resonant frequency of a circuit. At HF frequencies, relays can be used to switch capacitors, inductors or entire tuned circuits into and out of use. However, at higher frequencies, relays become unsuitable. Furthermore, relays have a relatively high current demand and are undesirable at any frequency for this reason.

Page 2, please replace the fourth full paragraph as follows:

According to the present invention, there is also provided an insulated gate field effect transistor comprising source and drain regions within a surrounding region and gate electrode means provided over a channel or channels between said source and drain region and over at least part of the boundary between said source and drain regions and said surrounding region, said surrounding region being provided with ground connection means for connection to an AC ground. The source and drain

regions are preferably n- or n^+-type within a p-type substrate region. If, however, the source and drain regions are p- or p^+-type, the substrate region may be an n-type region within a greater p-type region. If the source and drain regions are n+-type the surrounding region is n- or n+-type and if the source and drain regions are p- or p+-type the surrounding region is p- or p+-type. The ~~normalised~~ normalized substrate resistance of PMOS devices can be much lower than that for NMOS devices. Accordingly, when sized correctly PMOS devices can perform better that NMOS devices for switching tuning components.

Page 3, please replace the fourth and fifth paragraphs as follows:

~~Providing metallic~~ Metallic interconnections are provided between the sources and metallic interconnections between the drain regions and between the source regions of small insulated gate field effect transistor having multi-drain/multi-source topographies, e.g. the waffle structure.

Preferably, therefore the insulated gate field effect transistor includes a plurality of source and drain regions and an interconnection layer in which said source regions are connected together and said drain regions are connected together, the conductors of the interconnection layer being connected to said source and drain regions by splaying conductive paths. Splaying the connections in this way increases the spacing between the points which need to be interconnected in an interconnection layer.

Page 6, please replace the second full paragraph as follows:

Referring particularly to Figure 3b, a second metallisation layer comprises lateral conductor paths 38a, ..., 381 radiating from the tops of vias to respective peripheral source and drain regions 21, . .., 24, 26, 29. The corner conductor paths 38a, 38d, 38l, 38l extend diagonally away from the waffle. The other conductor paths 38b, 38c, 38e, 38f, 38g, 38h, 38j, 38k extend parallel to axes of the waffle and are broadened at their outer ends in the direction of the nearest corner conductor path 38a, 38d, 38i, 38l. The second metallisation layer also comprises pads 39 atop vias to the pads 37 of the first metallisation layer over the other source and drain regions 27, 28.

Page 7, please replace the first full paragraph as follows:

The ~~centre~~ center to ~~centre~~center separation of ~~neighbouring~~ neighboring pads 42 in the fourth metallisation layer is much greater than that of the underlying source and drain regions 21, ..., 24, 26, ..., 29 due to the radiating paths 38a, ..., 38l, 41 in the second and third metallisation layers, making formation of the first and second conductor patterns 43, 44 easier.

Page 8, please replace the first, second, third and fourth full paragraphs as follows:

Referring to Figure 6a, the capacitor switching arrangement of Figure 1 is applied to an LC tank circuit including an inductor ~~5141~~ connected in parallel with the first capacitor 10.

Referring to Figure 6b, the circuit of Figure 6a is modified by connecting a fourth capacitor ~~54~~44 between the drain and source of the MOSFET 11. Consequently, turning on of the MOSFET 11 increases the capacitance of the tank circuit, thereby decreasing the resonant frequency of the tank circuit

Referring to Figure 6c, the circuit of Figure 6a is modified by replacing the second and third capacitors 12, 13 with second and third inductors ~~52, 53~~42, 43.

Referring to Figure 6d, the circuit of Figure 6c is modified by connecting the second and third inductors ~~52, 53~~42, 43 in series and arranging to MOSFET 11 to selectively provide a short between taps on the second and third inductors ~~52, 53~~42, 43.